REMARKS

Claims 1-11 were previously pending in this application.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. No. 4,697,330 issued to Paterson et al ("Paterson").

Claim 11 is amended to correct a grammatical error.

New claims 12-13 are added.

No new matter is added.

Reconsideration is respectfully requested.

Claim Rejections – 35 USC § 102

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Paterson.

The rejection is respectfully traversed.

The Examiner argues that Paterson (col. 8, lines 1-68) teaches, among other things, "selectively removing the control gate conductive layer 38 and the *inter-gate dielectric layer* 28/30 which are located in the *peripheral* circuit region, thereby exposing the gate conductive layer 38/40 in the peripheral circuit region." (Emphasis added)

In the peripheral circuit region of the Paterson reference, however, only a second polycide layer 38/40 and a second gate oxide layer 36 are sequentially formed on a semiconductor substrate. Then, the second polycide layer 38/40 is patterned using a mask layer 42 to form a patterned structure, as shown in FIG. 6a of the Paterson reference.

Thus, nothing in Paterson teaches or discloses, "selectively removing ...the *inter-gate dielectric* layer 28/30, thereby *exposing the gate conductive* layer in the *peripheral* circuit region." If the second polysicide layer 38/40 is removed in the Paterson reference, merely the second gate oxide layer 36 would be exposed, not the gate conductive layer as recited in claim 1 of the present application. Alternatively, if the second polycide layer and the second gate oxide 36 are both removed in the Paterson reference, merely the bare semiconductor substrate would be exposed. See FIG. 6a of the Paterson reference.

For these reasons, Paterson does not teach or disclose all of the elements of claim 1. Thus, claim 1 is allowable. Also, claims 2-10, which depend from allowable claim 1 and recite features that are neither nor disclosed in the cited references, are allowable.

In addition, new claim 12 recites "stripping the control gate conductive layer and the inter-gate dielectric layer which are located in the peripheral circuit region to expose the gate

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

11. (Once amended) The method of claim 1, further comprising:

patterning the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and

patterning the gate conductive layer that [are] is located in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region.

Claims 12 and 13 are new.

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1	SRNT	1

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